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*Don E. Boag*

Applicant(s): John S. Yates, Jr., et al.  
Title: COMPUTER WITH TWO EXECUTION MODES

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JUL 07 2003

Mail Stop RCE  
Commissioner for Patents  
P.O. Box 1450  
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Technology Center 2100

**RESPONSE ACCOMPANYING RCE**

Kindly amend the application as follows.

**In the claims:**

- C1
- 1 1. (twice amended) A computer, comprising:
  - 2 a processor pipeline designed to alternately execute instructions coded for first and
  - 3 second different computer architectures or coded to implement first and second different
  - 4 processing conventions;
  - 5 a memory for storing instructions for execution by the processor pipeline, the
  - 6 memory being divided into pages for management by a virtual memory manager, a single
  - 7 address space of the memory having first and second pages;
  - 8 a memory unit designed to fetch instructions from the memory for execution by the
  - 9 pipeline, and to fetch stored indicator elements associated with respective memory pages of
  - 10 the single address space from which the instructions are to be fetched, each indicator element
  - 11 designed to store an indication of which of two different computer architectures and/or
  - 12 execution conventions under which instruction data of the associated page are to be executed